Listing of the Claims

A complete listing of the claims with proper claim identifiers is set forth below.

1. (Previously presented) A nonvolatile memory element having a conductivity state changeover material and two electrically conductive electrodes present at the conductivity state changeover material and serving for the application of a voltage and generation of an electric field in the conductivity state changeover material of at least two different conductivity states prevailing in the conductivity state changeover material, between which changeover can be repeatedly effected by the application of predetermined programming voltages, wherein at least one of the electrodes has at least one field amplification structure for amplifying a field strength of the electric field in the conductivity state changeover material.

2. (Previously presented) The nonvolatile memory element as claimed in claim 1, characterized in that the field amplification structure constitutes a projection of the electrodes which projects into the conductivity state changeover material.

3. (Previously presented) The nonvolatile memory element as claimed in claim 2, wherein the projection constitutes a tip, corner or edge of the electrodes.

4. (Previously presented) The nonvolatile memory element as claimed in claim 3, wherein an angle of the tip, corner or edge is ≤ 90 degrees.

5. (Previously presented) The nonvolatile memory element as claimed in claim 1, wherein the conductivity state changeover material has a hydrogen-saturated amorphous semiconductor material.

6. (Previously presented) The nonvolatile memory element as claimed in claim 1, wherein the conductivity state changeover material has a multilayer construction.

7. (Previously presented) The nonvolatile memory element as claimed in claims 1, wherein the electrodes have a metal.

8. (Withdrawn) A method for producing a nonvolatile memory element having the following steps:

a) preparation of a carrier material;

b) formation of an auxiliary layer;

c) formation of a depression in the auxiliary layer;

d) filling of the depression with a first electrically conductive material for forming a first electrode;

e) formation of at least one field amplification structure at the first electrode;

f) formation of a conductivity state changeover material on the first electrode with the field amplifier structure, after which at least two different conductivity states prevailing in the conductivity state changeover material, between which changeover can be repeatedly effected by the application of predetermined programming voltages; and

g) formation of a second electrically conductive electrode on the changeover material.

9. (Withdrawn) The method as claimed in claim 8, characterized in that, in step a), a semiconductor substrate is prepared as the carrier material.

10. (Withdrawn) The method as claimed in claim 8, wherein, in step a), a word line is formed in the carrier material in the region of the depression, the word line having a material which realizes an ohmic or diode junction with the material of the first electrode.

11. (Withdrawn) The method as claimed in claim 8, wherein, in step a), a selection transistor having source/drain regions is formed in the carrier material, the source/drain regions in each case realizing a bit line and a terminal region for the first electrode.

12. (Withdrawn) The method as claimed in claim 8, wherein, in step b), an insulator layer is deposited over the whole area on the carrier material.

13. (Withdrawn) The method as claimed in claim 8, wherein, in step c), a resist layer is formed and patterned; at least part of the auxiliary layer is removed using the patterned resist layer; the resist layer is removed; and a cleaning step is carried out.

14. (Withdrawn) The method as claimed in claim 13, cwherein, in step c), anisotropic etching is carried out for the at least partial removal of the auxiliary layer.

15. (Withdrawn) The method as claimed in claim 8, wherein, in step c), a trench or a hole is formed as the depression.

16. (Withdrawn) The method as claimed in claim 8, wherein, in step d), the electrically conductive material is deposited in such a way that an adapted depression is produced in a region of the depression.

17. (Withdrawn) The method as claimed in claim 16, wherein, in step e), ell) the electrically conductive material is etched back conformally at least as far as a surface of the auxiliary layer by anisotropic etching; and e12) the auxiliary layer is etched back essentially as far as a bottom region of the adapted depression by anisotropic etching.

18. (Withdrawn) The method as claimed in claim 8, wherein, in step e), e21) the electrically conductive material is caused to recede at least as far as a surface of the auxiliary layer by planarization; and e22) the auxiliary layer is etched back by a predetermined amount by selective etching.

19. (Withdrawn) The method as claimed in claim 8, wherein, in step e), e31) at least a predetermined amount of the electrically conductive material is removed in the depression by etching; e32) a formation of a thin conformal electrically conductive layer is carried out in such a way that an adapted depression

remains in the region of the depression; e33) the electrically conductive layer is etched back at least as far as the surface of the auxiliary layer by anisotropic etching; and e34) the auxiliary layer is etched back essentially as far as a bottom region of the adapted depression by anisotropic etching.

20. (Withdrawn) The method as claimed in claim 8, wherein, in step f), a single or multiple hydrogen saturated, amorphous semiconductor layer is deposited on the first electrode with the field amplification structure.

21. (Withdrawn) The method as claimed in claim 8,wherein, in step g), a Cr, Au, Al, Cu, NiCr, Ag, Ni, Mo, V, Co, Fe, W or Mn layer is deposited as the second electrode.

22. (Previously presented) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in claim 1 which are arranged in matrix form and can be addressed via bit lines arranged in column form and word lines arranged in row form, characterized in that a respective first electrode is electrically connected via a diode junction to a respective word line formed in a semiconductor substrate, and a respective second electrode for forming a respective bit line is patterned in strip form at the surface of an auxiliary layer.

23. (Previously presented) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in claim 1 which are arranged in matrix form and can be addressed via bit lines) arranged in column form and word lines arranged in row form, characterized in that a respective first electrode is electrically connected via an ohmic junction to a respective word line formed in a semiconductor substrate, and a respective second electrode for forming the respective bit line is patterned in strip form at the surface of an auxiliary layer.

24. (Previously presented) A memory element arrangement having a multiplicity of nonvolatile memory elements as claimed in claim 1 which are arranged in matrix form and can be addressed via bit lines arranged in column form and word

lines arranged in row form, characterized in that there is formed, each memory element, a selection transistor with a word line serving as control layer and a bit line serving as first source/drain region in the semiconductor substrate, a second source/drain region of the selection transistor being electrically connected to a first electrode of the memory element and a respective second electrode being at a common potential.